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(54) SOLID-STATE IMAGE PICKUP DEVICE AND METHOD FOR DRIVING THE SAME

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a MOS-type image sensor that can take an image produced by an optical signal with the whole light-receiving surface, can convert the optical signal into an electrical signal, and can output the electrical signal as an image signal to the outside.

SOLUTION: The MOS-type image sensor includes a light-receiving diode 111, having a light-receiving region that is formed on a substrate 11, and produces light-producing electric charges, when light is applied thereto; an insulating gate type field effect transistor 112 for detecting optical signals which is provided with a region 25 for accumulating the light-producing electric charges, outputs a threshold voltage modulated by the accumulation of the light-producing electric charges as an optical

signal, and is formed on the substrate 11; an electric charge carrying path for carrying the light-producing electric charges produced in the light-receiving region to the region 25; an electric charge discharging path for discharging the light-producing electric charges produced in the light-receiving region to the substrate 11; and a means 42 for controlling a potential barrier with respect to the light-producing electric charges of the electric charge discharging path.

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CLAIMS

[Claim(s)]

[Claim 1] The light-receiving diode equipped with the light-receiving field which generates an optical generating charge by the optical exposure formed on the substrate, The insulated gate field effect transistor for lightwave signal detection which is equipped with the are recording field of said optical generating charge, and outputs the threshold voltage modulated by are recording of an optical generating charge as a lightwave signal and which was formed on said substrate, The charge transfer path of transmitting the optical generating charge generated in said light-receiving field to said are recording field, The solid state camera characterized by having the charge blowdown path which discharges the optical generating charge generated in said light-receiving field to said substrate, and a means to control the potential barrier over said optical generating charge of said

charge blowdown path.

[Claim 2] the 1st well of one conductivity type formed in the reverse conductivity-type layer by which said light-receiving diode was formed on said substrate of one conductivity type -- with a field said 1st well -- the 2nd well of one conductivity type with which it has the reverse conductivity-type field formed in the surface of a field, and said insulated gate field effect transistor for lightwave signal detection was formed in said reverse conductivity-type layer -- with a field said 2nd well surrounded by the common-law marriage of a ring-like gate electrode and the gate electrode of the shape of this ring -- with the source field formed in the field said 2nd well surrounding the rim of the gate electrode of the shape of said ring -- with the drain field formed in the field It is in a field. the 2nd well under the channel field between said drain fields and said source fields, and said channel field -- It has the high concentration buried layer which has high impurity concentration higher than a field. said 1st and 2nd wells formed so that said source field might be surrounded -- said light-receiving field -- said 1st well -- a field -- containing -- the are recording field of said optical generating charge -- said high concentration buried layer -- it is -- said charge transfer path -- said 1st well -- a field and the 2nd well -- the solid state camera according to

claim 1 characterized by including a field.

[Claim 3] said 1st well -- with the overflow drain field of one conductivity type linked to said substrate which adjoins a field through said reverse conductivity-type layer It has the overflow drain gate which applied on said overflow drain field from on the edge field of a field, and was formed through gate dielectric film. said 1st well -- The path which reaches said overflow drain field is included. said charge blowdown path -- said 1st well -- pass said reverse conductivity-type layer from the edge field of a field -- A means to control the potential barrier over the optical generating charge of said charge blowdown path is a solid state camera according to claim 2 characterized by being said overflow drain gate.

[Claim 4] the inside of said charge blowdown path -- it is -- at least -- said 1st well -- pass said reverse conductivity-type layer from a field -- the solid state camera according to claim 3 characterized by forming the 1 conductivity-type field in the surface of a path which reaches said overflow drain field.

[Claim 5] the inside of said charge blowdown path -- it is -- at least -- said 1st well -- pass said reverse conductivity-type layer from a field -- the solid state camera according to claim 3 characterized by forming the reverse conductivity-type field

in the surface of a path which reaches said overflow drain field.

[Claim 6] said 1st well -- a field and the 2nd well -- between fields -- said 1st well -- a field and the 2nd well -- claim 2 characterized by forming the potential barrier over said optical generating charge in said charge transfer path by making a low-concentration 1 conductivity-type field intervene rather than a field thru/or a solid state camera given in any 1 of 5.

[Claim 7] said 1st well -- a field and said 2nd well -- a field -- mutual -- connecting -- and said 1st well -- the high impurity concentration of a field -- said 2nd well -- claim 2 characterized by forming the potential barrier over said optical generating charge in said charge transfer path by making it higher than the high impurity concentration of a field thru/or a solid state camera given in any 1 of 5.

[Claim 8] the inside of said charge transfer path -- said 1st well -- a field and said 2nd well -- claim 2 characterized by having a means to control the potential barrier over said optical generating charge of the field which connects a field thru/or a solid state camera given in any 1 of 5.

[Claim 9] said 1st well -- a field and said 2nd well -- a means for the field which connects a field to be said reverse conductivity-type layer, and to control the potential barrier over said optical generating charge said 1st well -- said 1st well

from the edge of the reverse conductivity-type field formed in the surface of a field -- the edge field of a field -- said reverse conductivity-type layer and said 2nd well -- pass the edge field of a field -- the solid state camera according to claim 8 characterized by being the transfer gate prepared through gate dielectric film on the path which reaches the edge of said drain field.

[Claim 10] the inside of said charge transfer path -- it is -- at least -- said 1st well -- pass said reverse conductivity-type layer from a field -- said 2nd well -- the solid state camera according to claim 9 characterized by forming the 1 conductivity-type field in the surface of a path which reaches a field.

[Claim 11] the inside of said charge transfer path -- it is -- at least -- said 1st well -- pass said reverse conductivity-type layer from a field -- said 2nd well -- the solid state camera according to claim 9 characterized by forming the reverse conductivity-type field in the surface of a path which reaches a field.

[Claim 12] The solid state camera characterized by making the configuration of claim 1 thru/or the solid state camera of 11 into one pixel, and coming to carry out two or more arrays of this pixel on said substrate.

[Claim 13] each charge blowdown path of two or more of said adjoining pixels -- both -- each of said 1st well -- the solid state camera according to claim 12

characterized by having a means to be prolonged from a field, and to be connected with said substrate by one place, and to control the potential barrier over said optical generating charge in said each charge blowdown path.

[Claim 14] Said two or more pixels are claim 12 characterized by being arranged by the train and the line, or a solid state camera given in any 1 of 13.

[Claim 15] The vertical-scanning signal actuation scanning circuit where said solid state camera supplies a scan signal to the gate electrode of said insulated gate field effect transistor for lightwave signal detection, The drain electrical-potential-difference actuation scanning circuit which supplies a drain electrical potential difference to the drain field of said insulated gate field effect transistor, The signal output circuit which memorizes the electrical potential difference of the source field of said insulated gate field effect transistor, and outputs the lightwave signal corresponding to the electrical potential difference of said source field further, The solid state camera according to claim 13 characterized by having the horizontal scanning signal input scanning circuit which supplies the scan signal which controls the timing which reads said lightwave signal.

[Claim 16] The lightwave signal based on said optical generating charge is read

using a solid state camera according to claim 14. the actuation approach of the solid state camera outputted as a video signal -- it is -- (a) -- about said all pixels The potential barrier of a path from said are recording field to [makes low the potential barrier of said charge blowdown path to the residual charge in said light-receiving field, and] said substrate to the residual charge in the are recording field of said optical generating charge is made low. (b) Sweep out the residual charge in said light-receiving field and the are recording field of said optical generating charge to said substrate at least, and rank second. (c) About said all pixels, form a potential barrier in said charge transfer path and said charge blowdown path to the optical generating charge in said light-receiving field, make said light-receiving field generate said optical generating charge by optical exposure, accumulate in it, and rank second to it. (d) While forming a potential barrier in said charge blowdown path to the optical generating charge in said light-receiving field, make low the potential barrier of said charge transfer path, transmit and accumulate said optical generating charge in said are recording field through said charge transfer path, and rank second. About all the pixels on a par with said line chosen for lightwave signal read-out corresponding to said optical generating charge While the potential barrier of said charge

blowdown path is made low while forming a potential barrier in said charge transfer path to the optical generating charge in said light-receiving field, and reading the threshold change of potential corresponding to the accumulated dose of said optical generating charge The optical generating charge generated in said light-receiving field is discharged from said light-receiving field to said substrate through said charge blowdown path. On the other hand, about all the pixels of said other lines other than said selected line While forming a potential barrier in the path from the are recording field of said optical generating charge to said substrate to the optical generating charge of said are recording field and accumulating said optical generating charge in said are recording field A potential barrier is formed in said charge transfer path to the optical generating charge generated in said light-receiving field. And discharge the optical generating charge which makes low the potential barrier of said charge blowdown path, and is generated in said light-receiving field to said substrate through said charge blowdown path, and actuation of (e) above (d) is repeated. The actuation approach of the solid state camera characterized by reading the lightwave signal incorporated by said pixel one by one about said all lines.

[Claim 17] After the actuation which is before actuation of the above (e) and

reads the threshold change of potential corresponding to the accumulated dose of said optical generating charge in the above (d) The optical generating charge accumulated in the are recording field of said (d1) optical generating charge is discharged about all the pixels on a par with said line. Subsequently (d2) The threshold change of potential in the condition of having discharged said optical generating charge is read from the are recording field of said optical generating charge. Subsequently (d3) The actuation approach of the solid state camera according to claim 16 characterized by reading the signal of the difference of the threshold change of potential corresponding to the accumulated dose of said optical generating charge, and the threshold change of potential in the condition of having discharged said optical generating charge from the are recording field of said optical generating charge.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the solid state camera using MOS mold image sensors and its actuation approach of the threshold voltage modulation technique used for a video camera, an electronic camera, an image input camera, a scanner, or facsimile in more detail about a solid state camera and its actuation approach.

[0002]

[Description of the Prior Art] Since semi-conductor image sensors, such as CCD

mold image sensors and MOS mold image sensors, are excellent in mass production nature, they are applied to almost all images input device equipment with progress of the detailed-ized technique of a pattern. MOS mold image sensors are improved taking advantage of the advantage that power consumption is small and can create a sensor component and a circumference circuit element by the same CMOS technology especially in recent years compared with CCD mold image sensors.

[0003] In view of the trend of such a world, the applicant for this patent improved MOS mold image sensors, performed patent application (Japanese Patent Application No. No. 186453 [ten to]) about the sensor component which has the carrier pocket (high concentration buried layer) 25 under the channel field of the MOS transistor for lightwave signal detection, and has acquired the patent (registration number No. 2935492). The MOS mold image sensors have the structure shown in patent drawing 8 . In the structure, as shown in drawing 8 , a unit pixel consists of MOS transistors for lightwave signal detection which adjoin light-receiving diode and light-receiving diode. light-receiving diode and the MOS transistor for lightwave signal detection -- the well of p mold -- it is connected by the field. In the MOS transistor for lightwave signal detection, a gate electrode

has the shape of a ring, the source field of n mold is formed in a center section, and the drain field of n mold is formed so that the periphery of a gate electrode may be surrounded. the well near a gate electrode lower part and the source field -- the hole pocket of p mold is prepared so that a source field may be surrounded in a field.

[0004] By the way, taking out the distorted video signal which stood it still by reading outside the signal which read the video signal to the transfer way, and was read to the later transfer way after turning off the whole surface simultaneous shutter without the mechanical shutter and receiving a video signal with light-receiving diode and which is not can do a CCD sensor. On the other hand, in the above-mentioned MOS mold image sensors, an image is captured with light-receiving diode with a focal plane mold shutter. And the video signal in which photo electric translation was carried out by a series of repeat actuation is taken out. For example, each electrode is made to impress and depletion-ize high reverse voltage at an initialization period, and the optical generating electron hole which remains in a hole pocket is made to emit. Make the light-receiving diode section produce an optical generating electron hole by optical exposure at an are recording period, and make it transmit to a hole

pocket, it is made to accumulate, and a lightwave signal is detected by detecting the threshold of the field-effect transistor for lightwave signal detection modulated in proportion to the accumulated dose of an optical generating electron hole at the read-out period.

[0005]

[Problem(s) to be Solved by the Invention] However, by the above-mentioned image incorporation method, when photoing a high-speed migration body, and when taking a photograph with the image sensors which have many pixels more, the problem that distortion arises is in an image for the time difference of the start of reading, and a reading end. This invention is created in view of the trouble of the above-mentioned conventional technique, it is the whole light-receiving side surface, and it incorporates the image by the lightwave signal simultaneously, and offers the MOS mold image sensors which can change the lightwave signal into an electrical signal, and can be taken out outside as a video signal, and its actuation approach.

[0006]

[Means for Solving the Problem] In order to solve the above-mentioned technical problem, this invention relates to a solid state camera. As a basic configuration

of that solid state camera The light-receiving diode equipped with the light-receiving field which generates an optical generating charge by the optical exposure formed on the substrate, The insulated gate field effect transistor for lightwave signal detection which is equipped with the are recording field of said optical generating charge, and outputs the threshold voltage modulated by are recording of an optical generating charge as a lightwave signal and which was formed on said substrate, It has the charge transfer path of transmitting the optical generating charge generated in said light-receiving field to said are recording field, the charge blowdown path which discharges the optical generating charge generated in said light-receiving field to said substrate, and a means to control the potential barrier over said optical generating charge of said charge blowdown path.

[0007] That is, as shown in drawing 2 (a), drawing 7 (a), and drawing 11 (a), it has the unit pixel 101 containing the insulated gate field effect transistor 112 for lightwave signal detection (MOS transistor) which adjoins the light-receiving diode 111 and the light-receiving diode 111. and the 1st well of p mold with which the light-receiving diode 111 was formed in n type layer 32a on the substrate 11 of p mold -- the 2nd well of p mold with which it was formed in fields

15a and 43, and MOS transistor 112 was formed in n type layer 32b on the substrate 11 of p mold -- it is formed in field 15b. moreover, the 2nd well under the channel field of MOS transistor 112 -- the high concentration buried layer (carrier pocket: are recording field of an optical generating charge) 25 which is in field 15b and accumulates an optical generating charge in the periphery of the source field 16 is formed.

[0008] furthermore, it is shown in drawing 2 (a), drawing 7 (a), drawing 9 , and drawing 11 (a) -- as -- the 1st well of p mold of the light-receiving diode 111 section -- the overflow drain field 41 of p mold connected with the substrate 11 of p mold on both sides of n type layer 32a is formed next to fields 15a and 43. moreover, the 1st well -- the overflow drain gates (OFDG: a means to control the potential barrier over an optical generating charge) 42, 42a, and 42b are formed through insulator layer 18a over the upper part of the overflow drain field 41 from the upper part of the edge field of fields 15a and 43. the lower part of the overflow drain gates 42, 42a, and 42b -- it is -- the 1st well -- low-concentration n mold field or p mold field (surface field) 17c which connects the impurity range 17 of n mold of the light-receiving diode 111 section and the overflow drain field 41 of p mold with the surface of the edge field of fields 15a and 43 and the

surface of n type layer 32a is formed. the 1st above-mentioned well -- pass n type layer 32a and the overflow drain field 41 from fields 15a and 43 -- the path which results in the substrate 11 of p mold constitutes a charge blowdown path, and when required, the potential barrier over the optical generating charge of a charge blowdown path is controlled by the overflow drain gates 42, 42a, and 42b.

[0009] especially, it is shown in drawing 8 and drawing 10 -- as -- the well of the light-receiving diode 111 section -- the 1st well which adjoins in the direction of a train (or line writing direction), or the direction of slant, holding so that field 15a may be gathered and located in a line with a row and column -- the common overflow drain field 41 is formed to field 15a. the 1st mutual well which and the overflow drain gates 42a and 42b adjoin in the upper part of the overflow drain field 41 -- it is prepared so that pons delivery of the field 15a may be carried out.

[0010] In the above-mentioned configuration, in order to control the flow of the optical generating charge to the carrier pocket 25, it has the following descriptions so that the potential barrier over an optical generating charge can be controlled by the charge transfer path of resulting [from a light-receiving field] in the carrier pocket 25. it is shown [1st] in drawing 2 (a) -- as -- a charge transfer path -- setting -- the 1st and 2nd wells -- Fields 15a and 15b are

characterized by being connected through low-concentration p mold field 15c.

[0011] it is shown [2nd] in drawing 7 (a) -- as -- the 1st well of the light-receiving diode 111 section -- a field 43 -- the 2nd well of the MOS transistor 112 section -- it is characterized by the high impurity concentration of p mold being high rather than field 15b. it is shown [3rd] in drawing 11 (a) -- as -- the 1st and 2nd wells -- field 15a and 15b are arranged on both sides of n type layer 32a -- having -- **** -- the transfer gate 44 -- the 1st well -- pass the upper part of n type layer 32a from the upper part of the edge field of field 15a -- the 2nd well -- it is prepared over the upper part of the edge field of field 15b. 17d (surface field) of low-concentration p mold fields is formed in the surface of n type layer 32a under the transfer gate 44. 17d of p mold fields could be prepared, but n type layer 32a may be exposed to a front face with the case.

[0012] Next, when a hole (electron hole) is used as the solid state camera, especially the optical generating charge of the above-mentioned structure, the actuation approach of the solid state camera of this invention is explained. First, initialization actuation is performed. The actuation which discharges an optical generating charge from a light-receiving field and the carrier pocket 25 at least about all pixels is made to perform in initialization actuation. That is, the potential

barrier of a path from the carrier pocket 25 to [makes the potential barrier of a charge blowdown path low to the residual charge in a light-receiving field, and] a substrate 11 to the residual charge in the carrier pocket 25 is made low, and the residual charge in a light-receiving field and the carrier pocket 25 is swept out.

[0013] Subsequently, it moves to are recording actuation. The actuation which accumulates an optical generating charge in all pixels is made to perform in are recording actuation. That is, a potential barrier is formed in a charge transfer path and a charge blowdown path to the optical generating charge in a light-receiving field, it is the whole light-receiving side surface, and the lightwave signal based on an image is incorporated simultaneously. Thereby, an optical generating charge is generated in a light-receiving field, and an optical generating charge is accumulated in a light-receiving field. Subsequently, while forming a potential barrier in a charge blowdown path to the optical generating charge in a light-receiving field, the potential barrier of a charge transfer path is made low, and an optical generating charge is transmitted to the carrier pocket 25.

[0014] Subsequently, it moves to read-out actuation. In read-out actuation, every [a party] and the lightwave signal by which photo electric translation was carried

out are read. for this reason, about all the pixels on a par with the line chosen for lightwave signal read-out based on an optical generating charge While forming a potential barrier in a charge transfer path to the optical generating charge in a light-receiving field about all the pixels on a par with the line chosen for lightwave signal read-out corresponding to an optical generating charge, the potential barrier of a charge blowdown path is made low, and the threshold change of potential corresponding to the accumulated dose of an optical generating charge is read. At this time, when light is being succeedingly received in the light-receiving field, the optical generating charge generated in a light-receiving field is discharged by the substrate 11 through a charge blowdown path from a light-receiving field. While forming a potential barrier in the path from the carrier pocket 25 to [pixels / all / of the line (non-choosing line) which is not chosen / to the optical generating charge of the carrier pocket 25] a substrate 11 on the other hand and accumulating the optical generating charge in the carrier pocket 25 While discharging to a substrate the optical generating charge which forms a potential barrier in a charge transfer path to the optical generating charge generated in a light-receiving field, and makes the potential barrier of a charge blowdown path low, and is generated in a light-receiving field through a charge

blowdown path, it is made for the optical generating charge in the carrier pocket 25 not to be revealed.

[0015] Thus, the lightwave signal corresponding to an optical generating charge is read one by one for every line. In addition, the lightwave signal contains the noise signal component by the residual carrier leading to a noise. Special actuation for removing a noise signal component may be performed. That is, as shown in drawing 4 , drawing 5 , and drawing 6 , in read-out actuation, following read-out actuation of the lightwave signal of a selection line, the potential grant condition to the pixel of a non-choosing line is left as it is, initializes the pixel of the selection line like the above, and reads succeedingly the threshold voltage in the condition of having initialized. And the signal of the difference of the threshold voltage in the condition of having initialized with the threshold voltage corresponding to the amount of optical generating charges is computed, and a net lightwave signal component is outputted as a video signal.

[0016] Below, operation and effectiveness of being done so by the above-mentioned configuration are explained. In the solid state camera of this invention, it has the charge blowdown path which discharges the optical generating charge generated in the light-receiving field to a substrate 11, and a

means to control the potential barrier over the optical generating charge of a charge blowdown path. concrete -- a charge blowdown path -- the 1st well of the light-receiving diode 111 -- pass n type layer 32a and the overflow drain field 41 from field 15a -- it is the path which results in a substrate 11. Moreover, a means to control a potential barrier is the overflow drain gate 42 prepared on the charge blowdown path.

[0017] Therefore, the flow of the optical generating charge which faces to a substrate 11 from a light-receiving field by the way which is the need is controllable. moreover, the 1st well of the light-receiving diode 111 among charge transfer paths section -- the 2nd well of field 15a and the MOS transistor section -- it is placed between connection fields with field 15b by low-concentration p mold field 15c.

[0018] low-concentration p mold field 15c -- the 1st and 2nd surrounding wells -- compared with Fields 15a and 15b, the potential to an electron hole becomes high. In this case, by adjusting relatively the electrical potential difference impressed to the gate electrode 19, and the electrical potential difference impressed to drain field 17a, it can adjust so that the potential of p mold field 15c may serve as an obstruction over an optical generating charge. Thereby, the

flow of the optical generating charge which goes to the carrier pocket 25 from a light-receiving field by the way which is the need is controllable.

[0019] furthermore, the 1st well of the light-receiving diode 111 section -- a field 43 -- the 2nd well of the MOS transistor 112 section -- the high impurity concentration of p mold is high rather than field 15b. the 2nd well with the lower high impurity concentration of p mold -- field 15b -- the 1st well with the higher high impurity concentration of p mold -- the potential to an optical generating charge becomes high rather than a field 43. In this case, by adjusting relatively the electrical potential difference impressed to the gate electrode 19, and the electrical potential difference impressed to drain field 17a, it can adjust so that that potential difference may serve as an obstruction over an optical generating charge. Thereby, the flow of the optical generating charge which goes to the carrier pocket 25 from a light-receiving field is controllable.

[0020] moreover, the 1st well -- field 15a and the 2nd well -- field 15b is connected through n type layer 32a, and the transfer gate 44 is formed through insulator layer 18b on the connection field. Of a case, 17d of low-concentration p mold fields may be formed in the surface of n type layer 32a under the transfer gate 44. The electrical potential difference impressed to the transfer gate 44 can

adjust so that the potential of the field may serve as an obstruction over an optical generating charge. Thereby, the flow of the optical generating charge which goes to the carrier pocket 25 from a light-receiving field is controllable.

[0021] In the actuation approach of the solid state camera this invention, the initialization period, the are recording period, and the read-out period are repeated in this order. Especially, in an initialization period and an are recording period, about all pixels, perform initialization and are recording to the carrier pocket 25, and it sets in read-out actuation. In case a lightwave signal is read from the pixel of a selection line, while making it the carrier which controlled the potential of a charge transfer path and the potential of a charge blowdown path, and was accumulated in the carrier pocket 25 of a non-choosing line not revealed It can make it possible to discharge to a substrate 11, without moving the optical generating charge which read and was generated in the light-receiving field working to the direction of the carrier pocket 25.

[0022] By this, it is the whole light-receiving side surface, and the image by the lightwave signal can be simultaneously incorporated to a solid state camera, the lightwave signal can be changed into an electrical signal, and it can take out to the exterior of a solid state camera as a video signal. in addition, the 1st and 2nd

wells -- when Fields 15a and 15b etc. are the conductivity types of the above and reverse (i.e., when the high concentration buried layer 25 is n mold), the high concentration buried layer 25 serves as an electron pocket (carrier pocket), and will accumulate an optical generating electron.

[0023]

[Embodiment of the Invention] Below, it explains, referring to a drawing about the gestalt of operation of this invention.

(Gestalt of the 1st operation) Drawing 1 is the top view showing the component layout in the unit pixel of the MOS mold image sensors which are the gestalten of operation of the 1st of this invention. Drawing 2 (a) is a sectional view which meets the I-I line of drawing 1 .

[0024] As shown in drawing 1 and drawing 2 (a), the light-receiving diode 111 and MOS transistor 112 for lightwave signal detection are adjoined and formed in the unit pixel 101. The n channel depression MOS transistor (an MOS transistor may only be called hereafter) is used as MOS transistor 112. The unit pixel 101 had the shape of a rectangle mostly, and is aslant suitable to the train or the line writing direction. Space is separated by the overflow drain field 41 of p mold although the unit pixel 101 is not separated especially within the party.

[0025] the well from which these light-receiving diode 111 and MOS transistor 112 differ, respectively -- a field, i.e., the 1st well, -- field 15a and the 2nd well -- it forms in field 15b -- having -- those wells -- Fields 15a and 15b are mutually connected through low-concentration p mold field 15c. the 1st well of the part of the light-receiving diode 111 -- field 15a constitutes a part of generating field of the charge by optical exposure. the 2nd well of the part of MOS transistor 112 -- field 15b constitutes the gate field to which the threshold voltage of a channel can be changed with the potential given to this field 15b.

[0026] the 1st well which n type layer 32a is formed on the substrate 11 of p mold, and was described above in the part of the light-receiving diode 111 as shown in drawing 2 (a) -- field 15a is formed on this n type layer 32a. moreover, the 1st well -- the impurity range (reverse conductivity-type field) 17 of n mold is formed in the surface of field 15a. In the part of MOS transistor 112, as shown in drawing 2 (a), the substrate 11 of p mold is thicker than light-receiving diode 111 part including p type layer 11a with high concentration. the well which n type layer (reverse conductivity-type layer) 32b is formed on that p type layer 11a, and was described above -- field 15b is formed on this n type layer 32b. a well -- the gate electrode 19 is formed in the front face of the upper semi-conductor

substrate of field 15b through gate dielectric film 18.

[0027] The gate electrode 19 has the shape of a ring. it is surrounded by the common-law marriage of the ring-like gate electrode 19 -- as -- a well -- the source field 16 is formed in the surface of field 15b. the rim of the ring-like gate electrode 19 is surrounded -- as -- and a well -- drain field 17a is formed in those surfaces over n type layer 32a from field 15b. In the light-receiving diode 111 side, drain field 17a extends and the impurity range 17 of the light-receiving diode 111 is formed. namely, the 1st and 2nd wells which connected mutually an impurity range 17 and drain field 17a -- it is formed in one so that most fields may start the surface of Fields 15a and 15b. In addition, when calling it a drain field, even if it is describing it as 17a below as a sign which shows a drain field, a field including an impurity range 17 may be meant.

[0028] The source field 16 and the field between drain field 17a turn into a channel field. In the usual operating voltage, in order to hold a channel field in the depression condition, n mold impurity of moderate concentration is introduced into a channel field, and channel dope layer 17b of n mold is formed in it. the well under the n type of channel dope layer 17b -- in field 15b, the carrier pocket (high concentration buried layer; are recording field of an optical

generating charge) 25 is formed so that the source field 16 may be surrounded. the carrier pocket 25 -- the 1st and 2nd wells of carrier pocket 25 periphery -- since high impurity concentration of p mold is made high compared with Fields 15a and 15b, the potential of the carrier pocket 25 interior becomes low to an optical generating electron hole among optical generating charges. Thereby, an optical generating electron hole can be brought together in this carrier pocket 25.

[0029] in addition, the 1st and 2nd wells -- low-concentration p mold field (1 conductivity-type field) 15c which intervenes among Fields 15a and 15b is formed in the field equivalent to the boundary parts of drain field 17a by the side of the light-receiving diode 111, and channel dope layer 17b. the 1st well -- field 15a, low-concentration p mold field 15c, and the 2nd well -- the path which results in the carrier pocket 25 turns into a charge transfer path from the light-receiving field which consists of field 15b.

[0030] furthermore, the next door of the overflow drain field 41 of p mold which has separated space as mentioned above -- n type layer 32a -- minding -- the 1st well of the light-receiving diode 111 section -- field 15a is prepared. The overflow drain field 41 is connected with the substrate 11, and while separating space, it has the function which discharges a superfluous optical generating

charge to a substrate 11.

[0031] the 1st well -- pass n type layer 32a and the overflow drain field 41 from field 15a -- the path which results in a substrate turns into a charge blowdown path. furthermore, the 1st well among charge blowdown paths -- the overflow drain gate 42 is formed through gate-dielectric-film 18a over the overflow drain field 41 upper part from the upper part of the edge field of field 15a. the bottom of the overflow drain gate 42 -- the 1st well -- low-concentration n mold field (surface field) 17c is formed over the surface of n type layer 32a from the surface of the edge field of field 15a. That is, n mold field 17c has connected the overflow drain field 41 and the impurity range 17. By the case, low-concentration p mold field may be used instead of low-concentration n mold field 17c.

[0032] Moreover, the above-mentioned element is covered with the insulator layer 26, and fields other than light-receiving aperture 24 of the light-receiving diode 111 are shaded by the metal layer (light-shielding film) 23 formed on the insulator layer 26. Next, with reference to drawing 2 (b), it is in a flat surface parallel to the front face from the overflow drain field to the carrier pocket 25, and the situation of change of the valence band (Ev) along an one direction and the situation of change of the valence band (Ev) which meets in the depth direction

from the carrier pocket 25 to a substrate 11 are explained. Drawing 2 (b) is drawing which meets the II-II line of drawing 2 (a) and in which showing the situation of change of the summit of a valence band (Ev). It is more slightly [than the source field 16 drain field 17a, and an impurity range 17] deep, and the path which results in the left-hand side carrier pocket 25 centering on the light-receiving field of a drawing shows the situation of change of the valence band within a charge transfer path (Ev), and the path which reaches the right-hand side overflow drain field 41 shows the situation of change of the valence band within a charge blowdown path (Ev).

[0033] the 1st well as a light-receiving field -- on left-hand side, a charge transfer path consists of fields 15 -- the 1st well under an impurity range 17 -- field 15a and low-concentration p mold field 15c -- the 2nd well under drain field 17a and channel field 17b -- the 2nd well under field 15b, the carrier pocket 25, and the source field 16 -- the 2nd well under field 15b, the carrier pocket 25, channel field 17b, and drain field 17a -- field 15b is arranged. moreover, the 1st well -- the 1st well under an impurity range 17 which constitutes a charge blowdown path from a field 15 on right-hand side -- field 15a, n type layer 32a, and the overflow drain field 41 are located in a line. In this case, the condition of impressing the

electrical potential difference also to no electrode and field is shown. moreover, the 1st and 2nd wells -- the summit of the valence band (Ev) in Fields 15a and 15b is made into reference level.

[0034] Between the light-receiving field and the carrier pocket 25, the field of an energy level respectively lower than reference level is formed of n type layer 32a between low-concentration p mold field 15c and the light-receiving field, and the overflow drain field 41. The field where this energy level is low serves as an obstruction to an optical generating electron hole. Moreover, in the carrier pocket 25 of high-concentration p mold, it is higher than reference level and the optical generating hole has become are easy to be collected.

[0035] By adjusting the electrical potential difference applied to the field of gate 19 and overflow drain gate 42 and others, the height of a potential barrier can be adjusted and migration of an optical generating electron hole to the carrier pocket 25 or the overflow drain field 41 can be controlled. Next, with reference to drawing 3 , the configuration of the whole MOS mold image sensors using the unit pixel of the above-mentioned structure is explained. Drawing 3 shows circuitry drawing of the MOS mold image sensors in the gestalt of operation of the 1st of this invention.

[0036] As shown in drawing 3 , these MOS mold image sensors have taken the configuration of a two-dimensional array sensor, and the unit pixel 101 of the above-mentioned structure is arranged by the direction of a train, and the line writing direction in the shape of a matrix. Moreover, the actuation scanning circuit 102 of a vertical-scanning signal (VSCAN) and the actuation scanning circuit 103 of a drain electrical potential difference (VDD) are arranged across the pixel field at the right and left.

[0037] the vertical-scanning signal supply lines (VSCAN supply line) 59a and 59b and every one ... have come out from the actuation scanning circuit 102 of a vertical-scanning signal for every line. It connects with the gate electrode 19 of MOS transistor 112 in all the unit pixels 101 to which each vertical-scanning signal supply lines 59a and 59b and ... are located in a line with a line writing direction. moreover, the drain electrical-potential-difference supply lines (VDD supply line) 61a and 61b and every one ... have come out from the actuation scanning circuit 103 of a drain electrical potential difference (VDD) for every line. It connects with drain field 17a of MOS transistor 112 for lightwave signal detection in all the unit pixels 101 to which each drain electrical-potential-difference supply lines 61a and 61b and ... are located in a

line with a line writing direction.

[0038] Moreover, the vertical output lines 60a and 60b and every one ... have come out for every train, and it connects with the source field 16 of MOS transistor 112 in each vertical output lines 60a and 60b and all the unit pixels 101 to which ... is located in a line in the direction of a train, respectively. Moreover, the source field 16 of MOS transistor 112 is connected with the pressure-up scanning circuit 108 through the pressure-up electrical-potential-difference supply lines 73a and 73b and ... for every train. the inside of the carrier pocket 25, and the 1st and 2nd wells -- the high tension for discharging the charge which remains in field 15a and 15b is supplied.

[0039] Furthermore, the source field 16 of MOS transistor 112 is connected with the signal output circuit 105 through the vertical output lines 60a and 60b and ... for every train. And the source field 16 is connected with the a pair of 1st and 2nd line memory which consists of a capacitor which is not illustrated in the signal output circuit 105. The 1st line memory is made to memorize the 1st source potential when the optical generating charge is accumulated in the carrier pocket 25, and the 2nd line memory is made to memorize the 2nd source potential after discharging an optical generating charge from the carrier pocket

25. And the electrical potential difference of the difference of the 1st and 2nd source potentials is outputted as a lightwave signal through the differential amplifier which is not illustrated. In addition, active loads, such as a constant current source, are not connected to the source field 16 with the gestalt of this operation.

[0040] Every one horizontal scanning signal (HSCAN) supply lines 72a and 72b have come out from the horizontal scanning signal (HSCAN) input scanning circuit 104 for every train. Each horizontal scanning signal (HSCAN) supply lines 72a and 72b are connected with the signal output circuit 105. The horizontal scanning signal (HSCAN) input scanning circuit 104 supplies a horizontal scanning signal in the signal output circuit 105 through each horizontal scanning signal (HSCAN) supply lines 72a and 72b, and controls the timing which outputs a lightwave signal.

[0041] Reading appearance of the video signal (Vout) which does not contain the noise component by residual charge which drove MOS transistor 112 of sequential ** each unit pixel 101, and is proportional to the amount of incidence of light with a vertical-scanning signal (VSCAN) and a horizontal scanning signal (HSCAN) is carried out from the signal output circuit 105. Next, according to

drawing 4 , drawing 5 , and drawing 6 , photodetection actuation of the solid state image pickup device with which a single string continued is explained briefly.

[0042] Drawing 4 shows the timing chart of each I/O signal for operating the MOS mold image sensors concerning this invention. moreover, the light-receiving diode [in / in drawing 5 and drawing 6 / each actuation] 111 and a well -- it is the mimetic diagram showing the situation of change of the energy level (Ev) of Fields 15a and 15b, the carrier pocket 25, the overflow drain field 41 and the energy band of those peripheries, especially the summit of a valence band.

[0043] in this case -- as MOS transistor 112 for lightwave signal detection -- the 2nd well of p mold -- the n channel depletion type MOS transistor formed in field 15b is used. Photodetection actuation is performed by repeating a series of processes which consist of initialization period (**** period)-are recording period-read-out period -. Here, explanation is begun from an initialization period for convenience' sake. In addition, the overflow drain field 41 presupposes that it is grounded throughout a series of actuation.

[0044] First, initialization actuation is performed. initialization actuation -- setting

-- all pixels -- the inside of the carrier pocket 25, and the 1st and 2nd wells -- the charge which remains in field 15a and 15b is discharged. that is, it is shown in drawing 4 -- as -- all pixels -- the potential (Vpd) of drain field 17a (impurity range 17) -- about 5 -- V -- carrying out -- and the potential (Vg) of the gate electrode 19 -- about 7 -- it is referred to as V. Moreover, let potential (Vofdg) of the overflow drain gate 42 be touch-down potential (zero potential). The potential of drain field 17a also reaches the source field 16 through a channel field.

[0045] the electrical potential difference which channel field 17b maintained switch-on with the electrical potential difference impressed to the gate electrode 19, and was impressed to the source field 16 and drain field 17a while the electrical potential difference took for the pn junction of drain field 17a, the source field 16, and an impurity range 17, and the pn junction by the side of a substrate 11 at this time -- the 2nd well -- field 15b and the hole pocket 25 are started. the high electric field which the field of the upper part of a substrate 11 is depletion-ized, and are generated by this at this time -- the 1st well of the light-receiving diode 111 section -- the 2nd well which contains the carrier pocket 25 while the residual electron hole in field 15a is directly discharged by the substrate 11 -- a residual electron hole is certainly discharged from field 15b.

moreover -- as shown in drawing 5 (b), even if it lets the low overflow drain field 41 of potential pass -- the well of the light-receiving diode 111 section -- the residual electron hole in field 15a is discharged.

[0046] Next, are recording actuation is performed. Also in this case, about all pixels, an optical generating electron hole is generated in a light-receiving field, and it is transmitted and stored up in the carrier pocket 25. About all pixels, an electrical potential difference (Vpd), for example, about 0.5 V, is impressed to drain field 17a of MOS transistor 112 for lightwave signal detection. gate voltage which a channel field does not depletion-ize to the gate electrode 19 to drain potential (Vpd) and source potential (Vps) and by which an electron is accumulated in it with sufficient electron density (Vg), about 2 [for example,], -- about V are impressed. [moreover,] the electrical potential difference (Vps) 0.5 [about] as an electrical potential difference (Vpd) with drain field 17a the electron of sufficient electron density for a channel field is accumulated by this, and the source field 16 is connected through drain field 17a and a channel field, and same with the source field 16 -- V is impressed. Furthermore, 3V (Vofdg) are impressed to the overflow drain gate 42.

[0047] gate voltage in which a channel field does not depletion-ize but an

electron is accumulated with sufficient electron density in an are recording period (Vg), about 2 [for example,], -- by impressing about V, the electron hole generating core of the interface state density in the interface of gate dielectric film 18 and a channel field is deactivated, and bleedoff of the electron hole from interface state density, i.e., leakage current, is controlled. Thereby, the are recording to the carrier pocket 25 of electron holes other than an optical generating charge is controlled, and the so-called generating of a white crack can be prevented in an image screen.

[0048] then, the light-receiving side of all pixels -- and light is irradiated simultaneously at the light-receiving diode 111. If an electronic-electron hole pair (optical generating charge) is generated by optical exposure, as shown in drawing 5 (c) The potential barrier over the electron hole of p mold field 15c in the path (charge transfer path) from the light-receiving field to the carrier pocket 25, And since the potential barrier over the electron hole of n type layer 32a in the path (charge blowdown path) from the light-receiving field to the overflow drain field 41 is expensive, an optical generating electron hole will be accumulated in the light-receiving diode 111 section.

[0049] Next, as shown in drawing 4 and drawing 5 (d), (e), and (f), the optical

generating electron hole of the light-receiving diode 111 section is transmitted and accumulated in the carrier pocket 25 by the three-stage about all pixels. for this reason, it is first shown in drawing 5 (d) -- as -- all pixels -- the potential (Vpd) of drain field 17a of MOS transistor 112 for lightwave signal detection -- about 0.5 -- having held the potential (Vofdg) of the overflow drain gate 42 to V 3V, respectively -- the potential (Vg) of the gate electrode 19 -- touch-down potential -- carrying out -- the well of a light sensing portion -- the well which has the carrier pocket 25 to field 15a -- the potential of field 15b is lowered.

[0050] then, the 2nd well which sets potential (Vpd) of drain field 17a to 3V, and has the carrier pocket 25, holding the potential (Vg, Vps, Vofdg) of the gate electrode 19, the source field 16, and the overflow drain gate 42 in the front condition -- the potential of field 15b -- the 1st well of a light-receiving field -- it lowers further relatively to field 15a.

[0051] the 2nd well which finally sets potential (Vpd) of drain field 17a to 5V, holding the potential (Vg) of the gate electrode 19 in the front condition, sets potential (Vofdg) of the overflow drain gate 42 to 5V, and has the carrier pocket 25 -- the potential of field 15b -- the 1st well of a light-receiving field -- it lowers further relatively to field 15a.

[0052] Next, read-out actuation is performed. Read the threshold voltage of each pixel, i.e., the lightwave signal by which photo electric translation was carried out, per party, the storage in the signal output circuit 105 is made to memorize, and it is made to output to the water Hiraide line of force 71 as a video signal succeedingly in this read-out period. First, about 2 V is outputted to output line 59a from the VSCAN actuation scanning circuit 102 to the gate electrode 19 of a selection line about all the pixels of the 1st line. Touch-down potential is outputted to output line 59b to the gate electrode 19 of a non-choosing line. On the other hand, a selection line and a non-choosing line maintain VDD actuation scanning-line 61a at about 3 V (it becomes the drain potential of MOS transistor 112). Moreover, a selection line and a non-choosing line make the overflow drain gate 42 touch-down potential.

[0053] At this time, the reversal field of low electric field is formed in a part of channel field of the carrier pocket 25 upper part in the pixel of a selection line, and a high electric-field field is formed in the remaining part of a channel field. The drain voltage-current property of MOS transistor 112 shows saturation characteristics. Thereby, the 1st line memory is charged and the threshold voltage (source potential VoutS) by which light modulation was carried out to the

1st line memory is memorized in the place which charge completed. Moreover, as the continuous line of drawing 6 (g) shows, since the potential of the overflow drain gate 42 is low, the obstruction over an optical generating electron hole does not exist in a charge blowdown path. For this reason, the optical generating electron hole generated by optical exposure in a light-receiving field is discharged by the substrate 11 through the overflow drain field 41.

[0054] On the other hand, in the pixel of a non-choosing line, as the dotted line of drawing 6 (g) shows, an energy level changes, and the potential of the carrier pocket 25 is lower. For this reason, the optical generating electron hole accumulated in the carrier pocket 25 is not revealed during read-out actuation of a selection line. Moreover, since the potential of the overflow drain gate 42 is low, the optical generating electron hole generated by optical exposure in a light-receiving field is discharged by the substrate 11 through the overflow drain field 41.

[0055] As mentioned above, the electrical potential difference (that is, noise voltage (VoutN) is called.) which originated in the charge by the optical generating electron hole besides the electrical potential difference only by the optical generating electron hole is also included in the read threshold voltage. In

order to remove this noise voltage from a lightwave signal, actuation which reads only noise voltage (VoutN) is succeedingly performed about the selection line which performed read-out actuation. That is, about 7 V is outputted to output line 59a from the VSCAN actuation scanning circuit 102 to the gate electrode 19 of a selection line. Output line 59b to the gate electrode 19 of a non-choosing line is held to touch-down potential. Moreover, a selection line and a non-choosing line maintain VDD actuation scanning-line 61a at about 5 V. Moreover, a selection line and a non-choosing line hold the overflow drain gate 42 with touch-down potential. By this, as the continuous line of drawing 6 (h) shows, an energy level changes, and in the pixel of a selection line, residual charge is discharged from the inside of a semi-conductor like the initialization actuation shown by drawing 5 (b).

[0056] On the other hand, in the pixel of a non-choosing line, as the dotted line of drawing 6 (h) shows, an energy level changes, and the potential of the carrier pocket 25 is lower. For this reason, the optical generating electron hole accumulated in the carrier pocket 25 is not revealed during read-out actuation of a selection line. Moreover, since the potential of the overflow drain gate 42 is low, the optical generating electron hole generated by optical exposure in a

light-receiving field is discharged by the substrate 11 through the overflow drain field 41.

[0057] Subsequently, by the pixel of a selection line, like the time of drawing 6 (g), as the continuous line of drawing 6 (i) shows, an energy level is changed, and MOS transistor 112 is operated. Thereby, the 2nd line memory is charged and the threshold voltage (source potential VoutN) in the condition that the optical generating electron hole is not accumulated in the carrier pocket 25 is memorized by the 2nd line memory in the place which charge completed. As the dotted line of drawing 6 (i) shows, an energy level is changed, and it is made for the optical generating electron hole accumulated in the carrier pocket 25 not to be revealed during read-out actuation of a selection line like the time of drawing 6 (g) in a non-choosing line on the other hand.

[0058] Then, as the continuous line of drawing 6 (j) shows, an energy level is changed, and actuation which outputs the electrical potential difference of the difference of the source potentials VoutS and VoutN is performed. Thus, the video signal (Vout=VoutS-VoutN) proportional to an optical dose can be taken out. Then, actuation of drawing 6 (g) thru/or drawing 6 (j) is repeated, and read-out actuation is performed for every party. In the meantime, in the

non-choosing line which is not yet reading, a condition [that an optical generating electron hole is accumulated in the carrier pocket 25] is held.

[0059] Thus, one image can be projected on a screen by reading the lightwave signal by which photo electric translation was carried out from the pixel of all lines. As mentioned above, in the actuation approach of the solid state camera which is the gestalt of implementation of the 1st of this invention, the initialization period, the are recording period, and the read-out period are repeated in this order. Especially, in an initialization period and an are recording period, about all pixels, perform initialization and are recording to the carrier pocket 25, and it sets in read-out actuation. In case a lightwave signal is read from the pixel of a selection line, while making it the optical generating charge which controlled the potential of a charge transfer path and the potential of a charge blowdown path, and was accumulated in the carrier pocket 25 of a non-choosing line not revealed It can make it possible to discharge from the overflow drain field 41, without the optical generating charge which read and was generated in the light-receiving field working moving to the direction of the carrier pocket 25.

[0060] By this, it is the whole light-receiving side surface, and the image by the lightwave signal can be simultaneously incorporated to image sensors, the

lightwave signal can be changed into an electrical signal, and it can take out to the exterior of image sensors as a video signal. Furthermore, in a series of processes of are recording actuation-read-out actuation-initialization actuation (********), since a charge generating field and a charge transfer field have an embedded structure, when an optical generating electron hole moves, the ideal photoelectrical translator which does not interact with the noise source in a semi-conductor front face or a channel field can be realized.

[0061] (Gestalt of the 2nd operation) Drawing 7 (a) is the sectional view of the solid state image pickup device which is the gestalt of the 2nd operation. Drawing 7 (b) is drawing showing the situation of change of the energy level (Ev) of the summit of the valence band which meets the III-III line of drawing 7 (a). a different place from drawing 2 (a) in drawing 7 (a) -- the 1st well -- field 15a and the 2nd well -- without it prepares low-concentration p mold field between field 15b -- the 1st well -- the high impurity concentration of p mold of field 15a -- the 2nd well -- it is the point made higher than the high impurity concentration of p mold of field 15b. In addition, among drawing, since what is shown with the sign as drawing 2 (a) with other same signs shows the same thing as drawing 2 (a), it omits explanation.

[0062] this shows drawing 7 (b) -- as -- the inside of a charge transfer path -- the 1st well -- field 15a and the 2nd well -- the potential barrier over an electron hole where potential becomes high can be formed in a boundary with field 15b so that an energy level may become low to the optical generating electron hole which goes to the carrier pocket 25 from a light-receiving field. Therefore, in are recording actuation of the optical generating electron hole shown in drawing 5 (c), it is possible to prevent migration of an optical generating electron hole to the carrier pocket 25 and the overflow drain field 41, and to store up an optical generating electron hole in a light-receiving field.

[0063] Initialization actuation, are recording actuation, and a series of actuation that consists of read-out actuation are repeatable like the gestalt of the 1st operation by this, it is the whole light-receiving side surface, and the image by the lightwave signal can be simultaneously incorporated to image sensors, the lightwave signal can be changed into an electrical signal, and it can take out to the exterior of image sensors as a video signal.

(Gestalt of the 3rd operation) Drawing 8 is the top view showing the component layout in the unit pixel of the MOS mold image sensors which are the gestalten of the 3rd operation. Drawing 9 is a sectional view which meets the IV-IV line of

drawing 8 .

[0064] In the gestalt of the 3rd operation, a different place from the gestalt of the 1st operation it is shown in drawing 8 -- as -- the 1st well of the light-receiving diode 111 section, holding so that field 15a may be gathered and located in a line with a row and column and the 1st well of the light-receiving diode 111 section which adjoins in the direction of a train (or line writing direction) -- it approaches in field 15a -- making -- preparing -- those 1st well -- it is the point that the overflow drain field 41 common to field 15a is formed. moreover, the mutual well which and overflow drain gate (OFDG) 42a adjoins in the upper part of the overflow drain field 41 -- it is the point established through gate-dielectric-film 18a so that pons delivery of the field 15a may be carried out.

[0065] As shown in drawing 9 , the configuration of the lower part of overflow drain gate 42a is characterized by having combined the same configuration as the configuration which reaches the impurity range 17 of the light-receiving diode 111 by two 2-ways centering on the square-like overflow drain field 41 from the overflow drain field 41 which can set caudad the overflow drain gate 42 of drawing 2 (a).

[0066] moreover, it is shown in drawing 8 -- as -- a unit pixel -- almost -- the

shape of a rectangle -- having -- the 1st well of the light-receiving diode 111 section -- it is the same as the gestalt of the 1st operation that the direction of the list of the gate electrode 19 of field 15a and MOS transistor 112 is suitable in the direction of slant to the direction of a train or a line writing direction. in order to fulfill the above-mentioned conditions on the other hand -- the 1st well of the light-receiving diode 111 section in a unit pixel -- the point which is reverse by the pixel by which the sense of the list of the gate electrode 19 of MOS transistor 112 adjoins field 15a differs from the gestalt of the 1st operation.

[0067] In addition, among drawing, since what is shown with the sign as drawing 2 (a) with other same signs shows the same thing as drawing 2 (a), it omits explanation. the gestalt of implementation of the above 3rd -- setting -- the 1st well of the light-receiving diode 111 section -- the 1st well of the light-receiving diode 111 section which adjoins in the direction of a train (or line writing direction), holding so that field 15a may be gathered and located in a line with a row and column -- it approaches in field 15a -- making -- preparing -- those 1st well -- the overflow drain field 41 common to field 15a is formed.

[0068] thereby -- the gestalt of the 1st operation -- differing -- especially -- the 1st well -- it becomes unnecessary to form the band-like overflow drain field 41

which connects both field 15a and which functions also as a diffusion isolation region over space Since other configurations are the same as that of the gestalt of the 1st operation, also in the gestalt of the 2nd operation, the same operation and effectiveness as the gestalt of the 1st operation can be done so.

[0069] (Gestalt of the 4th operation) Drawing 10 is the top view showing the component layout in the unit pixel of the MOS mold image sensors which are the gestalten of the 4th operation. Drawing 11 (a) is a sectional view which meets the V-V line of drawing 10 . In the gestalt of the 4th operation which is drawing showing the signs of change of the energy level (Ev) of the summit of a valence band that drawing 11 (b) meets the VI-VI line of drawing 11 (a) the 1st well of the light-receiving diode 111 section, holding so that field 15a may be gathered and located in a line with a row and column and the 1st well of the light-receiving diode 111 adjoining section -- it approaches in field 15a -- making -- preparing -- those 1st well -- the point that the overflow drain field 41 common to field 15a is formed is the same as the gestalt of the 3rd operation.

[0070] On the other hand, in the gestalt of the 4th operation, a different place from the gestalt of the 3rd operation is the point that the transfer gate (TG) 44 is established in the boundary part of drain field 17a by the side of the

light-receiving diode 111 which adjoins channel field 17b, and the impurity range 17 of the light-receiving diode 111 section through insulator layer 18b, as shown in drawing 11 (a). in this case, the 1st and 2nd wells -- field 15a and 15b are arranged on both sides of n type layer 32a under the transfer gate 44 -- having -- **** -- the transfer gate 44 -- the 1st well -- the 2nd well from the upper part of the edge field of field 15a -- it is prepared over the upper part of the edge field of field 15b. the 1st and 2nd wells -- Fields 15a and 15b are connected by 17d (surface field) of low-concentration p mold fields formed in the surface of n type layer 32a under the transfer gate 44.

[0071] The pixel to which a place which are other configurations in the gestalt of the 4th operation, and is different from the gestalt of the 3rd operation carries out the overflow drain field 41 in common is a point which are what are arranged in the direction of slant to the direction of a train, or a line writing direction. moreover, the 1st well -- it is the point that field 15a has the shape of an octagon. In addition, among drawing, since what is shown with the sign as drawing 2 (a) with other same signs shows the same thing as drawing 2 (a), it omits explanation.

[0072] moreover -- the above -- the 1st and 2nd wells -- although Fields 15a and

15b are connected by 17d of low-concentration p mold fields formed in the surface of n type layer 32a under the transfer gate 44, they are shown in drawing 12 -- as -- the 1st well -- field 15a and the 2nd well -- field 15b may be formed so that n type layer 32a may be inserted. as mentioned above, the gestalt of implementation of the 4th of this invention -- setting -- the inside of a charge transfer path -- the 1st well -- field 15a and the 2nd well -- on the connection field with field 15b, the transfer gate 44 is formed through insulator layer 18b.

[0073] Therefore, the electrical potential difference impressed to the transfer gate 44 can adjust so that the potential of the connection field may serve as an obstruction over an optical generating charge. Thereby, the flow of the optical generating charge which goes to the carrier pocket 25 from a light-receiving field by the way which is the need is controllable. Next, the actuation approach of the MOS mold image sensors a configuration of being shown in drawing 11 with reference to drawing 13 thru/or drawing 15 is explained. It is applicable similarly about the MOS mold image sensors which have the configuration of the periphery of the transfer gate 44 shown in drawing 12 .

[0074] Drawing 13 shows the timing chart of each I/O signal for operating the MOS mold image sensors shown in drawing 11 . moreover, the light-receiving

diode [in / in drawing 14 and drawing 15 / each actuation] 111 and a well -- it is the mimetic diagram showing the situation of change of the energy level (Ev) of Fields 15a and 15b, the carrier pocket 25, the overflow drain field 41 and the energy band of those peripheries, especially the summit of a valence band.

[0075] in this case -- as MOS transistor 112 for lightwave signal detection -- the 2nd well of p mold -- the n channel depletion type MOS transistor formed in field 15b is used. Next, according to drawing 13 , drawing 14 , and drawing 15 , photodetection actuation of the solid state image pickup device with which a single string continued is explained briefly. Photodetection actuation is performed by repeating a series of processes which consist of initialization period (**** period)-are recording period-read-out period -. Here, explanation is begun from an initialization period for convenience' sake. In addition, the overflow drain field 41 presupposes that it is grounded throughout a series of actuation.

[0076] First, initialization actuation is performed. pass actuation of drawing 14 (a) thru/or (d) in initialization actuation -- all pixels -- the inside of the carrier pocket 25, and the 1st and 2nd wells -- the charge which remains in field 15a and 15b is discharged. As shown in drawing 14 (a), the residual charge in a light-receiving

field is transmitted to the carrier pocket 25. that is, it is shown in drawing 13 -- as -- the potential (Vpd) of drain field 17a (impurity range 17) -- about 3 -- V -- carrying out -- and the potential (Vg) of the gate electrode 19 -- about 0 -- V -- carrying out -- the potential (Vtg) of the transfer gate (TG) 44 -- about 0 -- V -- carrying out -- the potential (Vofdg) of the overflow drain gate 42 -- about 3 -- it is referred to as V.

[0077] Subsequently, as shown in drawing 14 (b), the residual charge within a charge transfer path is transmitted to the carrier pocket 25. namely, having held the potential (Vpd) of drain field 17a (impurity range 17), the potential (Vg) of the gate electrode 19, and the potential (Vofdg) of the overflow drain gate 42 in the front condition, as shown in drawing 13 -- the potential of the transfer gate (TG) 44 -- about 3 -- it is referred to as V.

[0078] Then, as shown in drawing 14 (c), the potential (Vofdg) of the overflow drain field 41 is lowered. subsequently, it is shown in drawing 14 (d) -- as -- the inside of the carrier pocket 25, and the 1st and 2nd wells -- the charge which remains in field 15a and 15b is discharged. that is, it is shown in drawing 13 -- as -- all pixels -- the potential (Vpd) of drain field 17a (impurity range 17) -- about 6 -- V -- carrying out -- and the potential (Vg) of the gate electrode 19 -- about 8 -- it

is referred to as V. moreover, the potential (Vtg) of the transfer gate (TG) 44 -- about 8 -- it is referred to as V. Furthermore, let potential (Vofdg) of the overflow drain gate 42 be touch-down potential (zero potential). The potential (Vpd) of drain field 17a also reaches the source field 16 through a channel field.

[0079] the electrical potential difference (Vg) impressed to the gate electrode 19 while the electrical potential difference took for the pn junction of drain field 17a, the source field 16, and an impurity range 17, and the pn junction by the side of a substrate 11 at this time -- the 2nd well -- field 15b and the 2nd well -- n type layer 32b under field 15b is started. the high electric field which the field of the upper part of a substrate 11 is depletion-ized, and are generated by this at this time -- the 1st well of the light-receiving diode 111 section -- the 2nd well which contains the carrier pocket 25 while the residual electron hole in field 15a is directly discharged by the substrate 11 -- a residual electron hole is certainly discharged from field 15b. moreover -- as shown in drawing 14 (d), even if it lets the low overflow drain field 41 of potential pass -- the 1st well of a light-receiving field -- the residual electron hole in field 15a is discharged.

[0080] Next, are recording actuation is performed. As shown in drawing 14 (e) and (f), drawing 15 (a), and (b), about all pixels, are recording actuation

generates an optical generating electron hole in a light-receiving field, and transmits and stores it up in the carrier pocket 25. An electrical potential difference (Vpd), for example, about 1 V, is impressed to drain field 17a of MOS transistor 112 for lightwave signal detection. gate voltage which a channel field does not depletion-ize to the gate electrode 19 to drain potential (Vpd) and source potential (Vps) and by which an electron is accumulated in it with sufficient electron density (Vg), about 2 [for example,], -- about V are impressed. [moreover,] the electrical potential difference (Vps) 1 [about] as an electrical potential difference (Vpd) with drain field 17a the electron of sufficient electron density for a channel field is accumulated by this, and the source field 16 is connected through drain field 17a and a channel field, and same with the source field 16 -- V is impressed. Furthermore, 3V (Vofdg) are impressed to the overflow drain gate 42.

[0081] then, the light-receiving side of all pixels -- and light is irradiated simultaneously at the light-receiving diode 111. Since the potential barrier over the electron hole of n type layer 32a in the path (charge blowdown path) from the light-receiving field to the overflow drain field 41 is expensive as shown in drawing 14 (e) when an electronic-electron hole pair (optical generating charge)

is generated by optical exposure, an optical generating electron hole will be accumulated in the light-receiving diode 111 section. In addition, since the potential barrier over the electron hole of n type layer 32b in the path (charge transfer path) from the light-receiving field to the carrier pocket 25 is low somewhat, a part has some which begin to be transmitted to the carrier pocket 25.

[0082] Next, as shown in drawing 14 (f) and drawing 15 (a), the optical generating electron hole of the light-receiving diode 111 section is transmitted and accumulated in the carrier pocket 25 about all pixels in two steps. As shown in drawing 13 , first the potential (Vtg) of the transfer gate 44 to touch-down potential about all pixels For this reason, the potential (Vofdg) of the overflow drain gate 42 has been held [and] to 3V, respectively. the potential (Vpd) of drain field 17a of MOS transistor 112 for lightwave signal detection -- about 3, while raising to V the potential (Vg) of the gate electrode 19 -- touch-down potential -- carrying out -- the 1st well of a light-receiving field -- the 2nd well which has the carrier pocket 25 to field 15a -- the potential of field 15b is lowered. The potential distribution whose generating charge of a light-receiving field is made to go to the carrier pocket 25 through a charge transfer field from a

light-receiving field is formed by this, and an optical generating electron hole is led to the direction of the carrier pocket 25.

[0083] Then, holding the potential (Vpd) of drain field 17a, the potential (Vg) of the gate electrode 19, the potential (Vps) of the source field 16, and the potential (Vofdg) of the overflow drain gate 42 in the front condition, the potential (Vtg) of the transfer gate 44 is raised to 3V, and the electric field which make the optical generating electron hole in the middle of a charge transfer path go to the carrier pocket 25 are strengthened further.

[0084] Finally, let potential (Vofdg) of the overflow drain gate 42 be touch-down potential, holding the potential (Vpd) of drain field 17a, the potential (Vg) of the gate electrode 19, the potential (Vtg) of the transfer gate 44, and the potential (Vps) of the source field 16 in the front condition, as shown in drawing 13 . As shown in drawing 15 (b), the optical generating charge which remains to a light-receiving field is discharged through the overflow drain field 41 at a substrate 11 side.

[0085] subsequently, having held the potential (Vtg) of the transfer gate 44, the potential (Vps) of the source field 16, and the potential (Vofdg) of the overflow drain gate 42 in the front condition, as shown in drawing 13 after a charge

transfer -- the potential (Vpd) of drain field 17a -- about 1 -- V -- carrying out -- the potential (Vg) of the gate electrode 19 -- about 2 -- it is referred to as V. Next, read-out actuation is performed. Read the threshold voltage of each pixel, i.e., the lightwave signal by which photo electric translation was carried out, per party, the storage in the signal output circuit 105 is made to memorize, and it is made to output to the water Hiraide line of force 71 as a video signal succeedingly in this read-out period.

[0086] First, as shown in drawing 13 , potential (Vpd) of drain field 17a is set to 3V about all pixels, holding the potential (Vtg) of the transfer gate 44, and the potential (Vofdg) of the overflow drain gate 42 in the front condition. Furthermore, about all the selected pixels of the 1st line (selection line), while holding the potential (Vg) of the gate electrode 19 to about 2 V, let potential (Vg) of the gate electrode 19 of a non-choosing line be touch-down potential.

[0087] At this time, the reversal field of low electric field is formed in a part of channel field of the carrier pocket 25 upper part in the pixel of a selection line, and a high electric-field field is formed in the remaining part of a channel field. The drain voltage-current property of MOS transistor 112 shows saturation characteristics. Thereby, the 1st line memory is charged and the threshold

voltage (source potential VoutS) by which light modulation was carried out to the 1st line memory is memorized in the place which charge completed. Moreover, as the continuous line of drawing 15 (d) shows, since the potential of the overflow drain gate 42 is low, the obstruction over an optical generating electron hole does not exist in a charge blowdown path. For this reason, the optical generating electron hole generated by optical exposure in a light-receiving field is discharged by the substrate 11 through the overflow drain field 41.

[0088] On the other hand, in the pixel of a non-choosing line, as the dotted line of drawing 15 (d) shows, an energy level changes, and the potential of the carrier pocket 25 is lower. For this reason, the optical generating electron hole accumulated in the carrier pocket 25 is not revealed during read-out actuation of a selection line. Moreover, since the potential of the overflow drain gate 42 is low, the optical generating electron hole generated by optical exposure in a light-receiving field is discharged by the substrate 11 through the overflow drain field 41.

[0089] Then, as the continuous line of drawing 15 (e) shows, an energy level is changed, and actuation which outputs a source electrical potential difference (VoutS) is performed. Thus, the video signal (Vout=VoutS) proportional to an

optical dose can be taken out. Then, actuation of drawing 15 (d) thru/or drawing 15 (e) is repeated, and read-out actuation is performed for every party. In the meantime, in the non-choosing line which is not yet reading, a condition [that an optical generating electron hole is accumulated in the carrier pocket 25] is held.

[0090] Thus, one image can be projected on a screen by reading the lightwave signal by which photo electric translation was carried out from the pixel of all lines. In addition, above, unlike the gestalt of the 1st operation, actuation excluding noise voltage (VoutN) from a lightwave signal (VoutS) is omitted, but when required, actuation which reads the source potential in the condition of having initialized with the actuation which initializes the carrier pocket 25, i.e., noise voltage, after the actuation which reads the lightwave signal by the optical generating electron hole shown in drawing 15 (d) is performed like the gestalt of the 1st operation. And actuation which outputs the electrical potential difference of the difference of the source potentials VoutS and VoutN at the time of the actuation which reads a lightwave signal from the line memory shown in drawing 15 (e) is performed. Thus, the video signal (Vout=VoutS-VoutN) proportional to an optical dose can be taken out.

[0091] As mentioned above, also in the gestalt of implementation of the above

4th, the initialization period, the are recording period, and the read-out period are repeated in this order like the gestalt of the 1st operation. Especially, in an initialization period and an are recording period, about all pixels, perform initialization and are recording to the carrier pocket 25, and it sets in read-out actuation. In case a lightwave signal is read from the pixel of a selection line, while making it the carrier which controlled the potential of a charge transfer path and the potential of a charge blowdown path, and was accumulated in the carrier pocket 25 of a non-choosing line not revealed The optical generating charge which read and was generated in the light-receiving field working can make it possible to discharge to a substrate 11 through the overflow drain field 41, without moving to the direction of the carrier pocket 25.

[0092] By this, it is the whole light-receiving side surface, and the image by the lightwave signal can be simultaneously incorporated to image sensors, the lightwave signal can be changed into an electrical signal, and it can take out to the exterior of image sensors as a video signal. Moreover, about other 4th configuration of the gestalt of operation, since it is the same as that of the gestalt of the 1st operation, also in the gestalt of the 4th operation, the same operation and effectiveness as the gestalt of the 1st operation can be done so.

[0093] (Gestalt of the 5th operation) Drawing 16 is the top view showing the component layout in the unit pixel of the MOS mold image sensors which are the gestalten of the 5th operation. In the gestalt of the 5th operation, it differs from the gestalt of the 4th operation, and the gestalt of the 4th operation of the point that the overflow drain field 41 is formed for every pixel although it is the same, in that transfer gate 44a and the overflow drain field 41 are formed.

[0094] in addition, the inside of drawing and sign 42C -- the 1st well -- the overflow drain gate prepared over the overflow drain field 41 top from on the edge field of field 15a -- it is -- 17C -- the 1st well under overflow drain gate 42c -- it is low-concentration n mold field or low-concentration p mold field established in the surface of a field from the edge field of field 15a to the overflow drain field 41.

[0095] As mentioned above, in the gestalt of the 5th operation, since it has the same configuration as the gestalt of the 4th operation except the point that the overflow drain field 41 is formed for every pixel, also in the gestalt of the 5th operation, the same operation and effectiveness as the gestalt of the 4th operation can be done so. As mentioned above, although the gestalt of operation explained this invention to the detail, the range of this invention is not

restricted to the example concretely shown in the gestalt of the above-mentioned implementation, and modification of the gestalt of the above-mentioned implementation of the range which does not deviate from the summary of this invention is included in the range of this invention.

[0096] For example, although the line memory which consists of an input capacitor is directly linked with the source field 56 in a signal output circuit with the gestalt of the above-mentioned operation, a constant current source is connected to juxtaposition and it is good for line memory also as source follower connection. In this case, it is not necessary to prepare a switched capacitor circuit. moreover, the inside of n type layer 32a on the substrate 11 of p mold, and 32b -- the 1st and 2nd wells -- although Fields 15a and 15b are formed -- instead of [of n type layers 32a and 32b] -- the epitaxial layer of p mold -- n mold impurity -- introducing -- n type layer -- forming -- the inside of this n type layer -- the 1st and 2nd wells -- Fields 15a and 15b may be formed.

[0097] Furthermore, although the substrate 11 of p mold is used, the substrate of n mold may be used instead. In this case, what is necessary is just to reverse all of each class explained with the gestalt of the above-mentioned implementation etc., and the conductivity type of each field, in order to acquire the same

effectiveness as the gestalt of the above-mentioned implementation. In this case, the carrier which should be accumulated in the carrier pocket 25 is an electron among an electron and an electron hole.

[0098]

[Effect of the Invention] As mentioned above, in the solid state camera of this invention, it has the charge blowdown path which discharges to a substrate the optical generating charge generated in the light-receiving field, and a means to control the potential barrier over the optical generating charge of a charge blowdown path. Therefore, the flow of the optical generating charge which faces to a substrate from a light-receiving field by the way which is the need is controllable.

[0099] Moreover, it has a means to control the potential barrier over an optical generating charge also in the charge transfer path of transmitting the optical generating charge generated in the light-receiving field to the are recording field of the MOS transistor for lightwave signal detection. Thereby, the flow of the optical generating charge which goes to an are recording field from a light-receiving field by the way which is the need is controllable. In the actuation approach of the solid state camera this invention, initialization actuation, are

recording actuation, and read-out actuation are repeated in this order. Especially, in initialization actuation and are recording actuation, about all pixels, perform initialization and are recording to an are recording field, and it sets in read-out actuation. In case a lightwave signal is read from the pixel of a selection line, while making it the carrier which controlled the potential of a charge transfer path and the potential of a charge blowdown path, and was accumulated in the are recording field of a non-choosing line not revealed It can make it possible to discharge to a substrate, without moving the optical generating charge which read and was generated in the light-receiving field working to the direction of an are recording field.

[0100] By this, it is the whole light-receiving side surface, and the image by the lightwave signal can be simultaneously incorporated to a solid state camera, the lightwave signal can be changed into an electrical signal, and it can take out to the exterior of a solid state camera as a video signal.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the top view showing the component layout in the unit pixel of the MOS mold image sensors concerning the gestalt of operation of the 1st of this invention.

[Drawing 2] Similarly (a) is a sectional view which meets the I-I line of drawing 1 . (b), It is drawing which meets the II-II line of this drawing (a) and in which showing the situation of change of the summit of a valence band (Ev).

[Drawing 3] It is drawing showing the circuitry of the whole MOS mold image sensors of drawing 1 .

[Drawing 4] The timing chart of each I/O signal for operating the MOS mold image sensors concerning the gestalt of operation of the 1st of this invention is shown.

[Drawing 5] the light-receiving diode in each period of drawing 4 , and a well -- it is the mimetic diagram (the 1) showing the situation of change of the energy level (Ev) of a field, a carrier pocket, an overflow drain field and the energy band of the periphery, especially the summit of a valence band.

[Drawing 6] the light-receiving diode in each period of drawing 4 , and a well -- it is the mimetic diagram (the 2) showing the situation of change of the energy level (Ev) of a field, a carrier pocket, an overflow drain field and the energy band of the periphery, especially the summit of a valence band.

[Drawing 7] (a) is a sectional view showing the structure of the component in the unit pixel of the MOS mold image sensors concerning the gestalt of operation of the 2nd of this invention which meets the I-I line of drawing 1 . (b) is drawing which meets the III-III line of this drawing (a) and in which showing the situation of change of the summit of a valence band (Ev).

[Drawing 8] It is the top view showing the component layout in the unit pixel of the MOS mold image sensors concerning the gestalt of operation of the 3rd of this invention.

[Drawing 9] Similarly, it is the sectional view which meets the IV-IV line of drawing 8 .

[Drawing 10] It is the top view showing the component layout in the unit pixel of the MOS mold image sensors concerning the gestalt of operation of the 4th of this invention.

[Drawing 11] Similarly, it is the sectional view which meets the V-V line of drawing 10 .

[Drawing 12] It is the sectional view showing other configurations of the transfer gate and its periphery similarly.

[Drawing 13] The timing chart of each I/O signal for similarly operating the MOS mold image sensors shown in drawing 10 and drawing 11 is shown.

[Drawing 14] the light-receiving diode in each period of drawing 13 , and a well -- it is the mimetic diagram (the 1) showing the situation of change of the energy level (Ev) of a field, a carrier pocket, an overflow drain field and the energy band of the periphery, especially the summit of a valence band.

[Drawing 15] the light-receiving diode in each period of drawing 13 , and a well -- it is the mimetic diagram (the 2) showing the situation of change of the energy level (Ev) of a field, a carrier pocket, an overflow drain field and the energy band of the periphery, especially the summit of a valence band.

[Drawing 16] It is the top view showing the component layout in the unit pixel of the MOS mold image sensors concerning the gestalt of operation of the 5th of this invention.

[Description of Notations]

11 11a Substrate

15a and 43 the 1st well -- field

15b the 2nd well -- a field

15c p mold field (1 conductivity-type field)

16 Source Field

17 Impurity Range (Reverse Conductivity-Type Field)

17a Drain field

17b Channel dope layer

17c, 17d Surface field

18, 18a, 18b Gate dielectric film

19 Gate Electrode

25 Carrier Pocket (High Concentration Buried Layer; Are Recording Field of Optical Generating Charge)

32a, 32b n type layer (reverse conductivity-type layer)

41 Overflow Drain Field

42, 42a, 42b, 42c Overflow drain gate

44 44a Transfer gate

59a, 59b VSCAN supply line

60a, 60b Vertical output line

61a, 61b VSCAN supply line

62a, 62b VDD supply line

71 Water Hiraide Line of Force

72a, 72b HSCAN supply line

73a, 73b Pressure-up electrical-potential-difference supply line

101 Unit Pixel

102 VSCAN Actuation Scanning Circuit

103 VDD Actuation Scanning Circuit

104 HSCAN Input Scanning Circuit

105 Signal Output Circuit

107 Video-Signal Output Terminal

108 Pressure-Up Scanning Circuit

111 Light-receiving Diode

112 Insulated Gate Field Effect Transistor for Lightwave Signal Detection (MOS Transistor for Lightwave Signal Detection)